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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,582	06/04/2001	Mukesh K. Puri	1003-0558	2635

7590 06/02/2004

Intellectual Property Department
LSI Logic Corporation
Mail Stop D-106
1551 McCarthy Boulevard
Milpitas, CA 95035

EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

pg4

Office Action Summary	Application No.	Applicant(s)	
	09/872,582	PURI ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-13 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-13 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 04 June 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-13 are presented for examination.

Drawings

The drawings are objected to because descriptive labels other than numerical are needed for figures 1 and 2. See 37 CFR 1.84(o). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and *should not compare the invention with the prior art*.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

The disclosure is objected to because of the following informalities: In line 23 of page 9 "In the embodiment of Fig. 2, step 105 is answered...". As step 105 is illustrated in Figure 3, this should read either "In the embodiment of Fig. 3, step 105 is answered..." or "In the embodiment of Fig 2, step 105 of Fig. 3 is answered...".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-13 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for allowing an output of test data, does not reasonably provide enablement for testing a semiconductor memory. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims. The independent claims 1 and 11 are directed to a method and circuit for testing a semiconductor memory. However, these claims describe a method of getting test data to an output register as there is no test data applied and no criteria listed for passing or failing data. The claims are directed to a plurality of shift registers for serial outputting the digital data to be received by the output register, which also sends the same output data back into the same shift register.

Claims 2-10 and 11-13 are dependent on claims 1 and 11 and therefore inherit the 35 U.S.C. 112, first paragraph issues of the independent claims. Claims 9, 10, 12, and 13 will not be further considered on their merits.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, in lines 6-9, "...a *corresponding one* of the plurality of shift registers to be input back into the *corresponding shift register* in a same sequence as the digital data is output from the *corresponding shift register*." This language is unclear as to which shift register is 'corresponding' to another shift register. The specification defines the flare register as "essentially serial shift registers" (page 7 lines 15-16), although 'FLARE' registers commonly used in the art is an acronym for 'faulty location analysis and repair execution' or 'fault latching and repair execution'. However, this does not define a 'corresponding' shift register. Still, it is evident from the drawings that the output from the last shift register *element* in the serial chain is fed back into the first shift register *element* of the same serial chain (or flare register). This would also allow the sequence to remain the same.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the

elements. See MPEP § 2172.01. The omitted elements are: a selection means which determines which register of the plurality of registers is output.

Claims 2-10 are dependent on claim 1 and therefore inherit the 35 U.S.C. 112, second paragraph issues of the independent claim. Claims 9 and 10 will not be further considered on their merits.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 8, and 11, are rejected under 35 U.S.C. 102(b) as being anticipated by Abramovici et al. in "*Digital Systems Testing and Testable Design*" IEEE Press 1990.

As per claims 1 and 11, Figure 10.9 (a) shows a feedback register which outputs the same sequence that is reloaded back in the same sequence (page 433).

As per claims 2-5 Abramovici et al teach that an n bit register will cycle through at most n states and that if the cycle length is k then the sequence would repeat every k clock cycles regardless the length of the shift chain (page 432 section 10.6.1 paragraph 2 and 3).

As per claim 8, it would be inherent to have a selector element (switch or multiplexer) in order to clock the data out of the plurality of registers.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 6-7, rejected under 35 U.S.C. 103(a) as being unpatentable over Abramovici et al. in "*Digital Systems Testing and Testable Design*" IEEE Press 1990.

As per claims 6 and 7, having a plurality of shift registers being output to an output register, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have made sure that the output register would be large enough to hold the amount of data that would be sent, and that at some point the output would be strobe in order to collect the data. This would have been obvious

because a person having ordinary skill in the art would want to access all of the data that had been collected.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,065,134 Bair et al.

This patent teaches repairing defective memory lines in an ASIC memory fabricated with redundancy rows and I/O memory lines. The method employs progressive urgency and dynamic repair schemes to attain optimal system performance in repairing defective memory lines in a memory array within an ASIC memory. This patent also teaches the use of a flare register.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/cb/
Cynthia Britt
Examiner
Art Unit 2133

/Guy J. Lamarre for/
Albert DeCady
Primary Examiner